selecting transistors are prepared for the respective drive TFTs and sequentially turned on by means of a Y-axis shift register so that the line-selecting transistors connected to each line are simultaneously turned on.

Page 2, first and second full paragraphs

According to such a device, since each of the column-selecting transistors has to drive all the drive TFTs on that column, it is necessary to use as a high power transistor for this column-selecting transistor. Particularly, in case that the light emissive elements are constituted by high speed elements such as EL elements, high speed switching operation will be required by using extremely high power TFTs.

These high power TFTs for the column-selecting transistors result in a time constant, determined by their large gate capacitance and on-resistance of circuits connected to the gates of the column-selecting transistors, to extremely increase and thus cause rise edges and fall edges of selection signals, applied to these respective gates, to delay by a certain period Δ T. Therefore, a selection signal to be applied to one column-selecting transistor will overlap on a next selection signal to be applied to the next column-selecting transistor for the delay time Δ T causing both of the neighboring column-selecting transistors to simultaneously keep on during this period Δ T. As a result, a video signal for light emissive element positioned at a certain column and a certain line will stray into a next light element positioned at the neighboring column and the same line causing picture quality of the display device to deteriorate.

Page 6, second full paragraph through page 8, first partial paragraph

Light emitting operation of the picture element P_{11} for example will be carried out as follows. When a selection signal x1 is output from the X-axis shift register 12 and a selection signal y1 is output from the Y-axis shift register 13, a column-selecting transistor (TFT) T_{x1} and a line selecting transistor (TFT) T_{y11} are turned on. Thus, the video signal -VL is applied to a gate of a drive transistor (TFT) M_{11} via the transistors T_{x1} and T_{y11}. Accordingly, a current with a value depending upon the gate voltage -VL flows from the EL power supply through drain and source of the drive transistor M_{11} causing

an EL element EL_{11} of this picture element P_{11} to emit light with a luminance corresponding to the voltage of the video signal -VL.

At a next timing, the X-axis shift register 12 turns off the selection signal x1 and outputs a selection signal x2. However, since the preceding gate voltage of the transistor M_{11} is held by a capacitor C_{11}, the picture element P_{11} will keep emitting light with a luminance corresponding to the voltage of the video signal -VL until this picture element P_{11} is selected again.

Fig. 3 shows a concrete constitution of a part of the X-axis shift register 12 in the embodiment of Fig. 1.

In the figure, two input NAND circuits 21 and 22 constitute a wave-form shaping circuit for shaping a wave-form of an input signal to synchronize with basic clocks. The NAND circuit 21 is connected such that inverse basic clocks -CL having inverted phase with respect to the basic clocks are input into one input terminal of the NAND circuit 21 and that an output signal from the NAND circuit 22 is input into the other input terminal thereof. The NAND circuit 22 is connected such that a start pulse -SP with low level (L-level) will be input into one input terminal of the NAND circuit 22 and that an output signal from the NAND circuit 21 is input into the other input terminal thereof. The start pulse -SP is an X-axis synchronous signal which defines a start time of scanning toward the column direction.

The output terminal of the NAND circuit 21 is connected to an input terminal of a clock inverter 26. This clocked inverter 26, clocked inverters 29 to 32 and inverters 33 to 37 constitute a shift register portion. Namely, each of the stages of the shift register portion is formed as follows. The first stage is constituted by the clocked inverter 26, the inverter 33 connected to this clocked inverter 26 in series and the clocked inverter 29 connected to the inverter 33 in parallel but in an opposite direction. The second stage is constituted by the clocked inverter 27, the inverter 34 connected to this clocked inverter 27 in series and the clocked inverter 30 connected to the inverter 34 in parallel but in the opposite direction. The third stage is constituted by this clocked inverter 28, the inverter 35 connected to this clocked inverter 28 in series and the clocked inverter 31 connected to the inverter 35 in parallel but in the opposite direction.

On page 9, first full paragraph continuing through first full paragraph on page 13

Third input terminals of the NAND circuits 23 to 25 are connected to a mask signal generation circuit 51 shown in Fig. 4 to receive a mask signal -INL. An output terminal of the NAND gate 23 is coupled with a gate of a first column switching transistor T_{x1} via the inverter 41. An output terminal of the NAND gate 24 is coupled with a gate of a second column switching transistor T_{X2} via the inverter 42. An output terminal of the NAND gate 25 is coupled with a gate of a third column switching transistor T_{x3} via the inverter 43. Into sources of the switching transistors T_{x1} to T_{x3}, video signal -VL is applied.

The clocked inverter will be in active and operate as an inverter when an L-level signal is applied to a clock input terminal shown at an upper side and also a H-level signal is applied to an inverted clock input terminal shown at a lower side. Contrary to this, it will turn into a high impedance state when the H-level signal is applied to the clock input terminal and the L-level signal is applied to the inverted clock input terminal. For example, since the clocked inverters 26 and 29 are constituted to receive opposite phase clocks with each other as shown in Fig. 3, the clocked inverter 26 will be in active when the clocked inverter 29 is in a high impedance state.

Fig. 4 schematically shows a constitution of a clock signal and mask signal generation circuit, Fig. 5 shows a concrete constitution of a mask signal generation circuit illustrated in Fig. 4, and Fig. 6 illustrates waveforms of a clock signal and a mask signal in the circuit of Fig. 4.

As shown in Fig. 4, the clock signal and mask signal generation circuit consists of a frequency divider 50 for dividing, by eight, frequency of a clock signal with eight-fold frequency, produced by a clock generator (not shown) to produce a basic clock signal CL, and a mask signal generation circuit 51 for producing a mask signal -INL from the clock signal with eight-fold frequency.

The frequency divider 50 may be constituted by a counter for counting the input clock signals to output the basic clock signal with H-level and L-level which alternate at every four input clock signals. Thus, the basic clock CL will have eight-fold pulse width in comparison with that of the input clock signal with eight-fold frequency as shown in Fig. 6.

As shown in Fig. 5, the mask signal generation circuit 51 consists of a three-bit counter 510 and a two-input NAND circuit 511 so as to count the input clock signal with eight-fold frequency for three clock cycles and provide an output signal with a one clock cycle duration of a L-level. Thus, the mask -INL having a predetermined mask period of time MK can be obtained. As will be apparent from Fig. 6, this mask period MK is equal to a quarter of a half clock cycle. The mask period MK according to this invention is not limited to a quarter of a half clock cycle but can be determined to an optional period equal to or longer than an overlapped period Δ T of the selection signals. In practice, it is desired to select the mask period MK between about 5 and 50% of the half clock cycle.

Fig. 7 illustrates waveforms of various signals in the X-axis shift register of Fig. 3. Hereinafter, operation of this embodiment will be illustrated in detail.

Output voltage A from the wave-form shaping circuit will be maintained at H-level when the start pulse of L-level -SP is not input. When the start pulse of L-level is input, the voltage A falls to L-level. As shown in Fig. 7, the start pulse -SP which is somewhat delayed due to a possible capacitance of input lead wires is shaped by the wave-form shaping circuit (21, 22) to synchronize with the basic clock CL.

When the voltage A falls to L-level, state of the clocked inverter 26 changes into active and thus output voltage B from the clocked inverter 26 will rise to H-level. Output voltage C from the inverter 33 (output from the first stage of the shift register) has an opposite phase waveform as that of the voltage B due to the inverter 33.

When the state of the clocked inverter 26 changes into high impedance in next, since the clocked inverter 29 is in active, the voltage B is kept on H-level during this active period of the clocked inverter 29. Namely, the inverter 33 and the clocked inverter 29 constitutes a hold circuit.

Output voltage D from the clocked inverter 27 has a waveform delayed by a half clock cycle from that of the voltage B due to the operations of the clocked inverter 27 itself which simultaneously changes into active state with the clocked inverter 29 and of a hold circuit constituted by the inverter 34 and the clocked inverter 30.

Output voltage E from the inverter 34 (output from the second stage of the shift register) has an opposite phase waveform as that of the voltage D due to inverter 34 and also has a waveform delayed by a half clock cycle from that of the voltage C.

Output voltage F from the clocked inverter 28 has a waveform delayed by a half clock cycle from that of the voltage D due to the operations of the clocked inverter 28 itself which simultaneously changes into active state with the clocked inverter 30 and of a hold circuit constituted by the inverter 35 and the clocked inverter 31.

Output voltage G from the inverter 35 (output from the third stage of the shift register) has an opposite phase waveform as that of the voltage F due to the inverter 35 and also has a waveform delayed by a half clock cycle from that of the voltage E.

The voltage C is inverted by the inverter 38 and an inverter voltage H which is maintained H-level for a clock cycle is applied to a first input terminal of the three input NAND circuit 23. The voltage E having a waveform delayed by a half clock cycle from that of the voltage C is applied to a second input terminal of the NAND circuit 23. The mask signal -INL is applied to a third input terminal of the NAND circuit 23. The mask period MK of the mask signal -INL is determined to a certain period so that the falling edge of the selection signal x1 and the rising edge of the next selection signal x2 will not overlap with each other.

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The voltage E is inverted by the inverter 39 and an inverted voltage I which is maintained at a H-level for a clock cycle is applied to a first input terminal of the three input NAND circuit 24. The voltage G having a waveform delayed by a half clock cycle from that of the voltage E is applied to a second input terminal of the NAND circuit 24. The mask signal -INL is applied to a third input terminal of the NAND circuit 24.

On page 14, third full paragraph

The voltage G is inverted by the inverter 40 and an inverter voltage J which is maintained H-level for a clock cycle is applied to a first input terminal of the three input NAND circuit 25. The voltage having a waveform delayed by a half clock cycle from that

of the voltage G is applied to a second input terminal of the NAND circuit 25. The mask signal -INL is applied to a third input terminal of the NAND circuit 25.

On page 15, fourth full paragraph continuing on page 16

As described before, the waveforms of these selection signals x1, x2, x3, . . . shown in Fig. 7 by solid lines are ideal waveforms and actual waveforms applied to the respective gates of the transistors T_{x1}, T_{x2}, T_{x3}, . . . may be as shown in Fig. 7 by broken lines. Namely, rising edges and falling edges of the selection signals may delay by a certain period Δ T due to the large gate capacitance of the transistors T_{x1}, T_{x2}, T_{x3}, . . . and on-resistance of the inverters 41, 42, 43, . . .

However, according to the present invention, since the mask period MK during which no H-level signal exists is provided between the selection signals, the switching transistor for example T_{x1} and the next switching transistor for example T_{x2} can never simultaneously be in an on state.

IN THE ABSTRACT:

Please replace the Abstract with the following:

An active matrix type flat-panel display device includes a flat substrate, a plurality of light emissive elements arranged two dimensionally along columns and lines on the flat substrate, a plurality of selection switches formed on the flat substrate, for sequentially selecting the light emissive elements to provide video signals thereto, selection signal generation circuits for providing selection signals which drive the selection switches in sequence so as to two dimensionally scan the light emissive elements, and a selection signal control circuit for preventing the selection signals from being output from the selection signal generation circuits for a predetermined period of time so as to eliminate overlap between the selection signals.